Development of a Hardened 150nm Standard Cell Library

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OUTLINE

SMDH
Santa Maria Design House

- Santa Maria Design House (SMDH)
- Background
- Hardening Techniques
  - Choosing the Target
  - Process Considerations on TID
  - Circuit Level
  - Layout Level
- SMDH RH Library
- NanoSatC-BR1
- NanoSatC-BR2
- SMDH RH Library: The future

Santa Maria Design House History

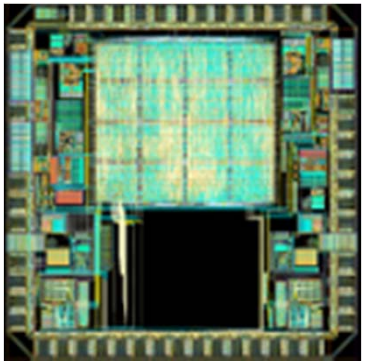
- GMicro 2001
- ADC_UCP Project 2006-2007
- TV Digital/UFSM 2008-2009
- Design flow and SMDH development July 2009
- Public call CNPq 59/2008: 12 new DHs (3 SP, 2 PE, 2 SC, 1 MG/DF/RJ/RS/AM) 2009

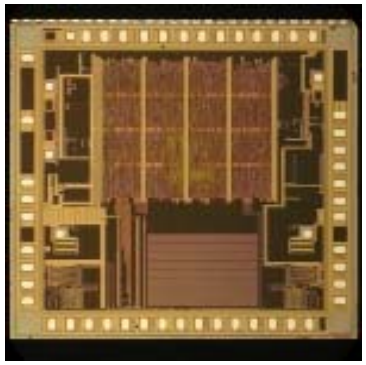
Santa Maria Design House Mission

Develop innovative solutions in electronic technology, for national and international markets.

Santa Maria Design House Solutions Microelectronics

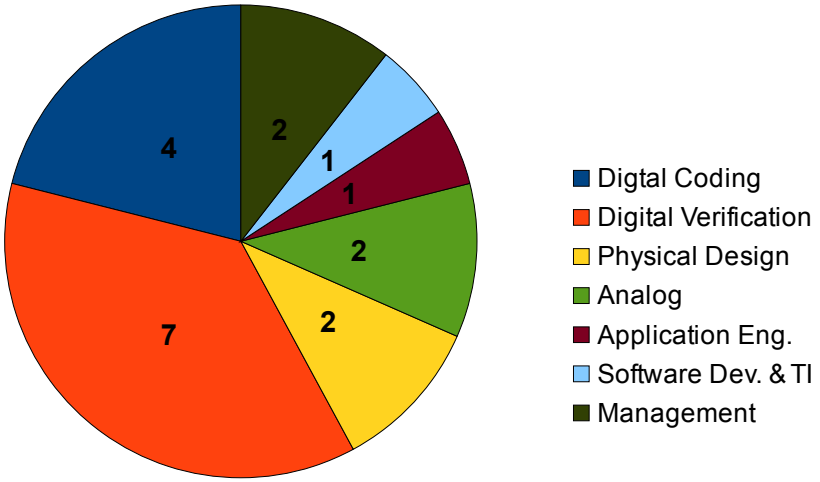
- Application Specific Integrated Circuits (ASICs)
- Systems on a Chip (SoCs)
- FPGA programming
- IPs development



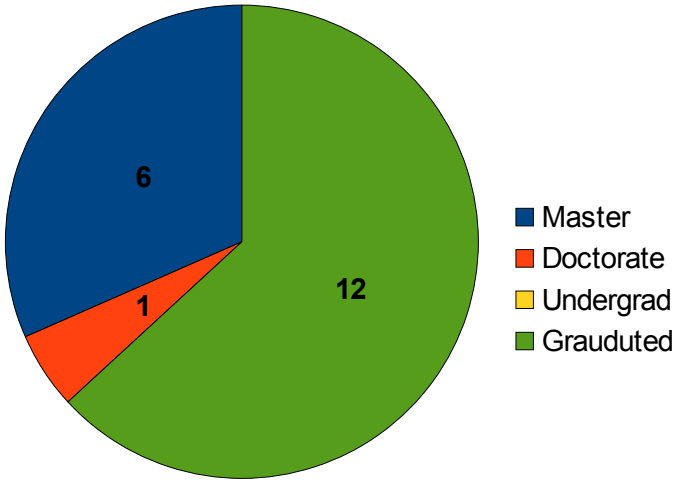


Santa Maria Design House Team

Knowledge Area

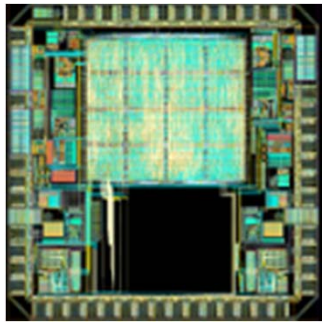


Academic Level



Total – 19 Engineers

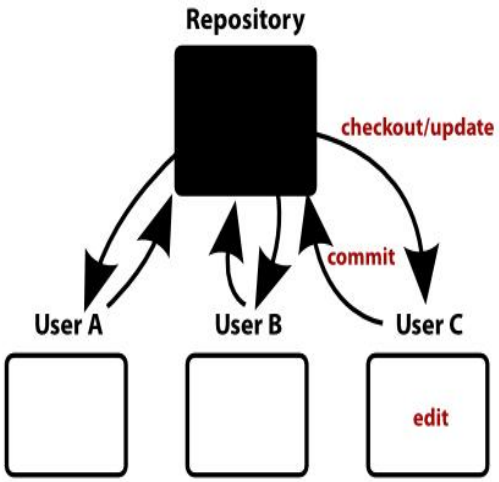
Santa Maria Design House Product Flow

Specification Design	Prototyping	Integration	Production
SMDH Santa Maria Design House	SMDH Santa Maria Design House	SMDH Santa Maria Design House	SMDH Santa Maria Design House
Customer		**Customer**	
	**Partner (Foundry)**		**Partner (Foundry)**

FABLESS

Santa Maria Design House Engineering Best Practices

- Version control
- Well-documented processes
- Automated design flow
- Post mortem process
- Entire CADENCE flow

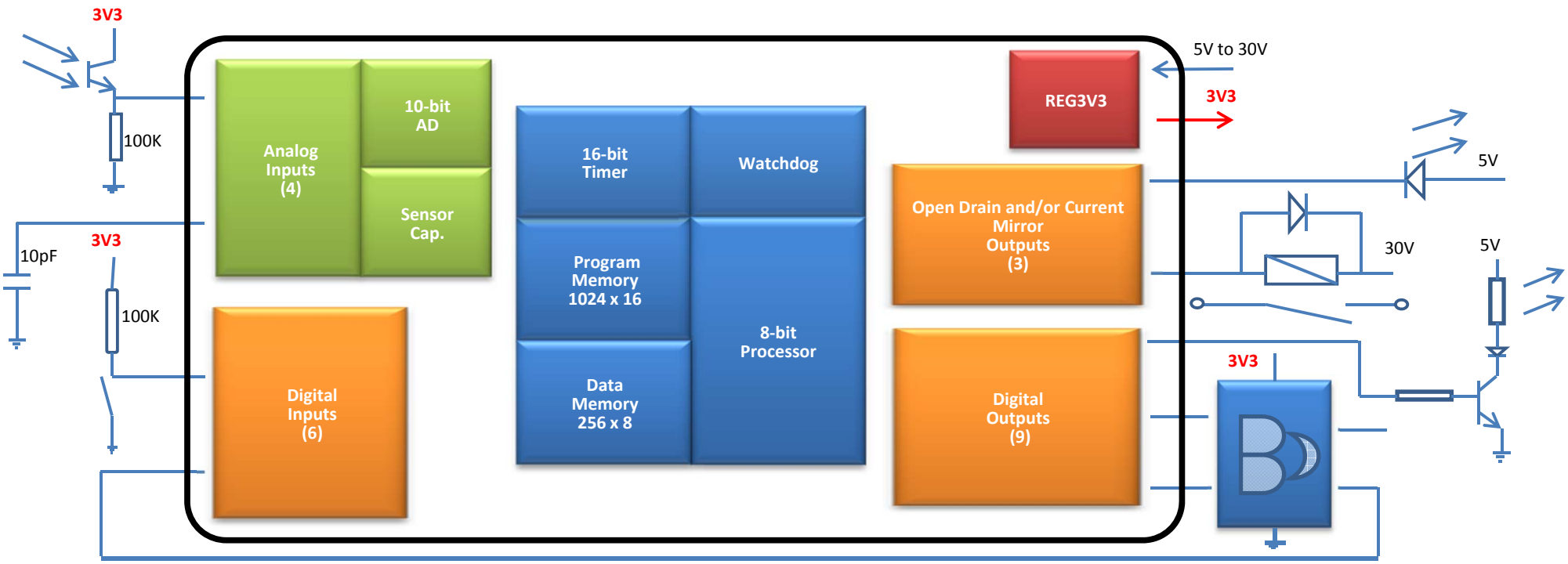


Santa Maria Design House Projects

SMDH Santa Maria Design House

Design	Technology	Digital (kgates)	Analog (mm2)	Status	End Date (mm/yy)
ZR16SO8 Microcontroller - 8 bits	XFAB XH035	37	2,0	Ready to production	out-15
ZR16LPO8 Microcontroller - 8 bits	XFAB XH035	37	2,0	Production test	jan-16
ZR16S08 Microcontroller – 16 bits	?	150	?	Codification	jun-16
SMDH_LIBV1 Radiation Hardened Cell Library	LFoundry LF150	0,1	0,0	Inside nanosat In the space	jun-14
SMDH_LIBV2 Radiation Hardened Cell Library	XFAB XH018	0,1	0,0	Ready	mai-15
Radiation Hardened on/off driver (digital only)	XFAB XH018	0,1	0,0	Ready	oct-15
PCI x Mil 1553 bridge	XH035	50	-	Release to Mectron	oct-15
ZR16RH08 Radiation Hardened microcontroller - 8 bits	XH018	35	-	Physica Design	dec-15

Application Diagram



Performance: ~ 4 MIPS
Power: ~ 6 mW

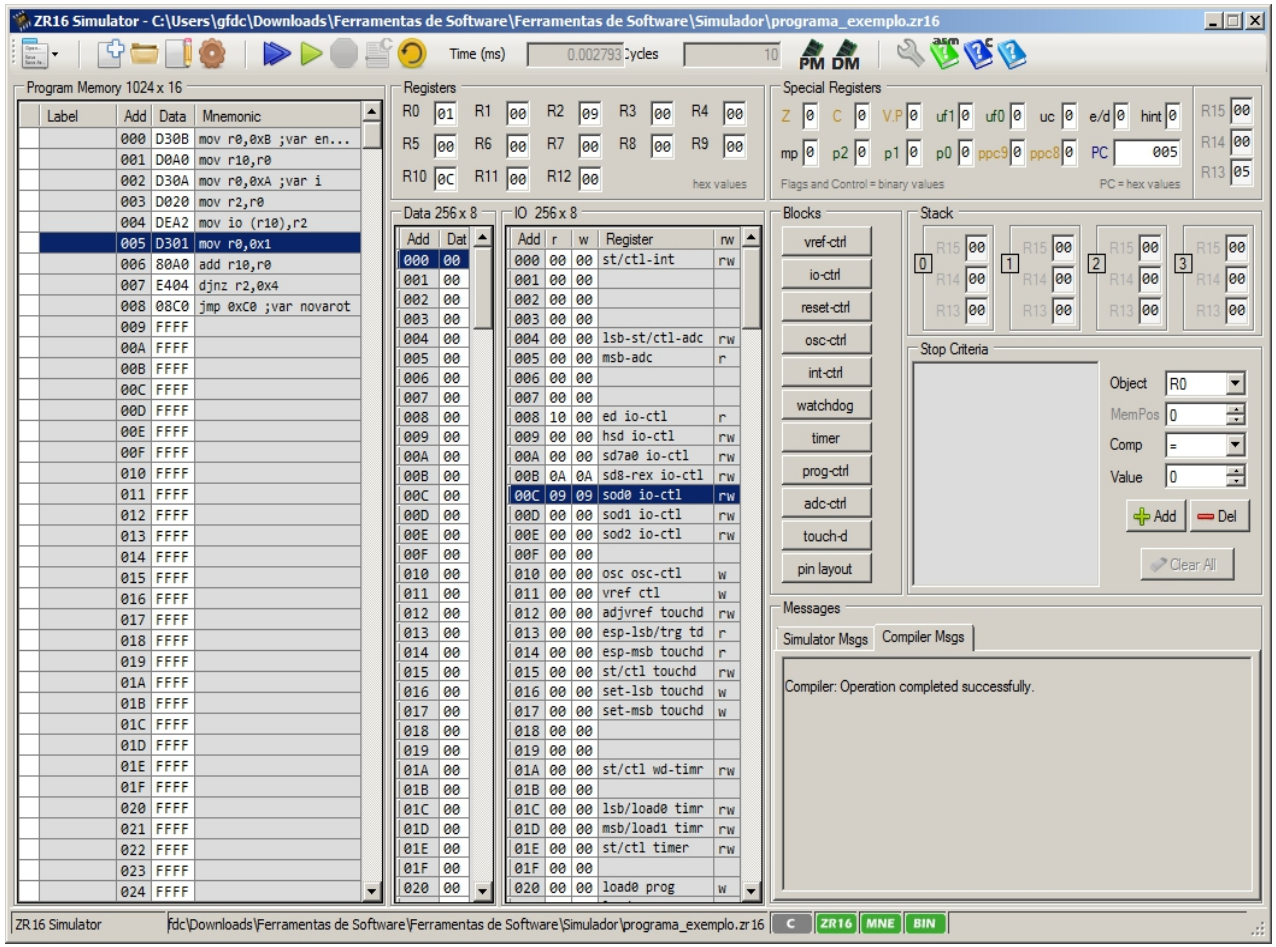
ZR16 Microcontroller -Features

- 8 bits RISC microprocessor
- 24 instructions
- 16 registers, 13 general purpose registers
- 4 position stack depth
- Program memory : 1024 x 16
- Data memory: 256 x 8
- internal oscillator , system clock 4MHz

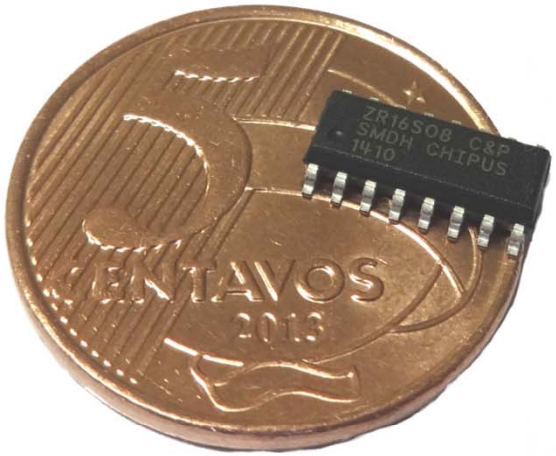
ZR16 Microcontroller - Features

- ❑16 bits timer
- ❑Watchdog
- ❑ 10 bits ADC @ 50KPS, 4 channels
- ❑Capacitive sensor
- ❑ Internal voltage regulator: 5V up to 30 V
- ❑3 open drain/current mirror output
- ❑9 digital output / 6 digital input
- ❑2 external interrupt input

ZR16 Microcontroller -Simulator



ZR16 Microcontroller - Pilot Lot



JC_14 set.pdf - Adobe Reader

Arquivo Editar Visualizar Documento Ferramentas Janela Ajuda

8 (1 de 1) 107% Localizar

Affonso Ritter

Observador

aritter20@gmail.com

O Papa e as cooperativas

Quais os diferenciais de uma cooperativa de outra entidade? Segundo o Papa Francisco, são sete. Ele os relacionou ao receber sábado em audiência sete mil membros da Banca Cooperativa de Roma. 1) Que desenvolva a parte mais fraca das comunidades locais e da sociedade civil. 2) Que se preocupe com a "relação entre a economia e a justiça social" tendo no centro "sempre a pessoa e não o dinheiro". 3) Que facilite e incentive a vida familiar. 4) Que proponha "soluções para a gestão cooperativa". 5) Que promova a "solidariedade e o uso social do dinheiro". 6) Que seja honesta para difundir a honestidade contra a corrupção. 7) E que participe ativamente no processo de globalização, porque "globalização é solidariedade".

Eventos de música

A Estação Musical de Porto Alegre lembra em grande estilo

INOVAÇÃO

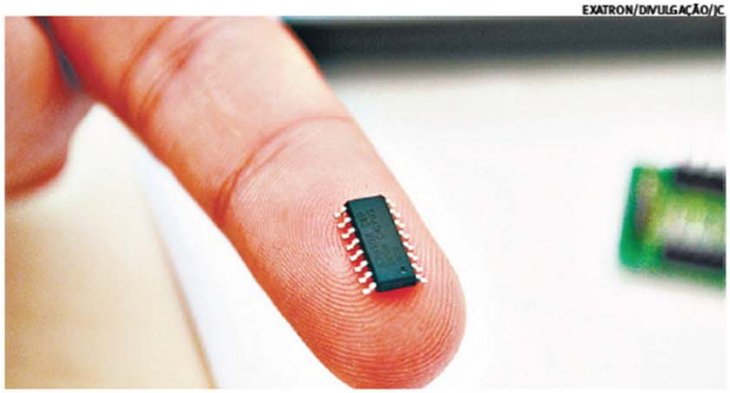
Relé fotocontrolador da Exatron tem chip nacional

Produto foi desenvolvido em parceria entre empresas e universidades

Patricia Knebel
patricia.knebel@jornaldocomercio.com.br

Depois de quatro anos de pesquisa e desenvolvimento, a gaúcha Exatron se prepara para lançar no mercado o primeiro relé fotocontrolador com chip brasileiro. Esse tipo de dispositivo faz a leitura da luminosidade de uma determinada rua e, ao detectar que está baixa, liga a luz automaticamente

EXATRON/DIVULGAÇÃO/JC



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MINISTÉRIO DA CIÊNCIA, TECNOLOGIA E INOVAÇÃO
GABINETE DO MINISTRO

Ofício nº 653/MCTI

Brasília, 25 de setembro de 2015

A Sua Magnificência o Senhor
Prof. PAULO AFONSO BURMANN
Reitor da Universidade Federal de Santa Maria – UFSM
Santa Maria - RS

Assunto: **Relé Fotocontrolador**

Senhor Reitor,

Incumbiu-me o Senhor Ministro de Estado da Ciência, Tecnologia e Inovação, Aldo Rebelo, de informar a Vossa Magnificência de que o MCTI recebeu com muita satisfação a comunicação da Universidade Federal de Santa Maria – UFSM, referente ao desenvolvimento do Microcontrolador ZR16S08 no Brasil, circuito integrado nacional, e que passará a integrar o Relé Fotocontrolador destinado ao controle de iluminação, produzido pela Exatron Produtos Inteligentes, empresa beneficiária da Lei de Informática.

2. O MCTI parabeniza especialmente as duas "design houses" do Programa CI-Brasil deste Ministério: Santa Maria Design House – SMDH e a Chipus Microeletrônica Ltda, esta última uma empresa beneficiária do Programa de Apoio ao Desenvolvimento da Indústria de

ofcio ministro.pdf

Mostrar todas as transferências...

ZR16 Microcontroller - Roadmap

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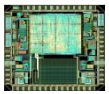
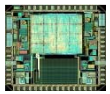
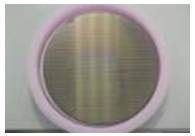


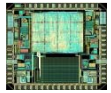
S08 Design



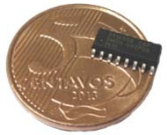
S08 Prototype



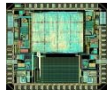
S08 Pilot Lot



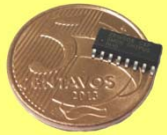
LP08 Design



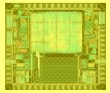
S08 Field Tests



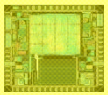
LP08 Prototype



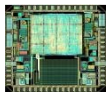
SO8 Release for Production



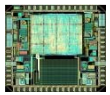
LP08 Production Tests



S16 Design



LP08 Release for Production



S16 Prototype

2011 | **2012** | **2013** | **2014** | **2015** | **2016**

Location and Contact

SMDH
Santa Maria Design House

Company headquarters –
Campus UFSM
Rua Q, Prédio 67
Santa Maria

Integrated Circuits (IC) design division
Fundação de Apoio à Tecnologia e Ciência
(FATEC–UFSM)

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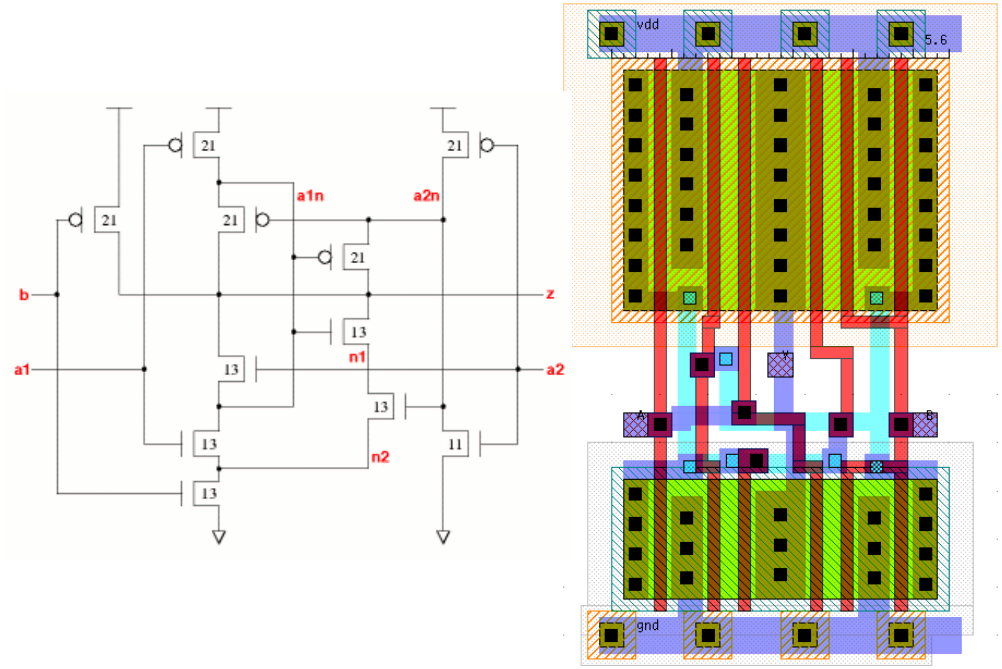
What is a standard cell library?

- Reusable cells becomes mandatory to implement full custom digital designs.
- Standard cells contains a set of logic primitives (for example AND,INV,OR,flip-flops) to recreate the desirable logic function.
- Standard cell share a regularized physical structure.
- Typically the standard cells are provided by the Foundry.



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Why use commercial IC technologies for radiation applications?

- Low cost/ high yield solution
- High speed and performance
- Low power
- Advanced nodes implement thin-gate oxide -> high TID tolerance

Standard cell implementation

- Use standard design flow and tools
- Provides highest density -> Highly sensitive to SEL & SEE
- Requires implement Radiation Hardening By Design approaches

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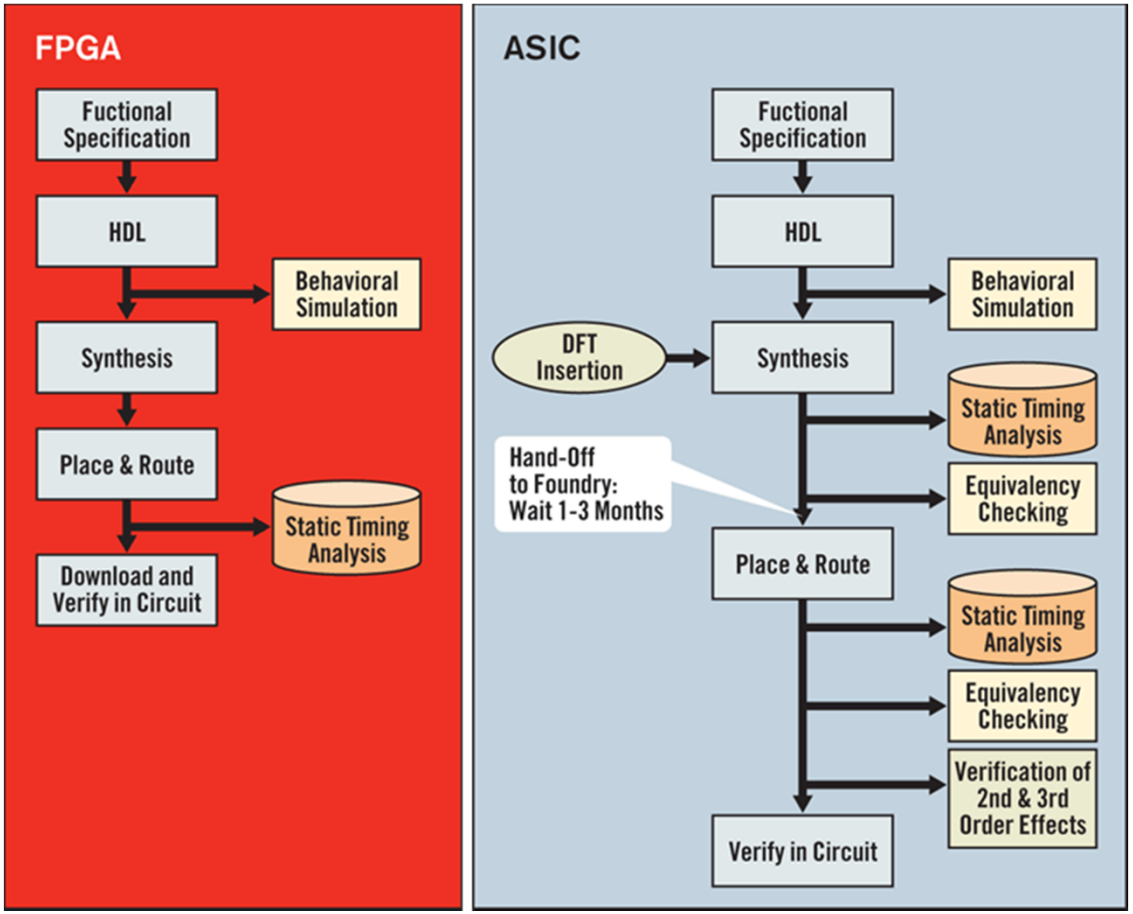
FPGA vs. ASIC implementation:

- **FPGA implementation:**
  - Faster time-to market.
  - No upfront non-recurring expenses (NRE).
  - Simpler design cycle.
  - Field reprogramability.
- **ASIC implementation:**
  - Full custom capability.
  - Allows to create System on Chips (SoC).
  - Smaller form factors.
  - More degrees of freedom to implement RHBD techniques.



Reference: FPGA vs. ASIC http://www.xilinx.com/fpga/asic.htm

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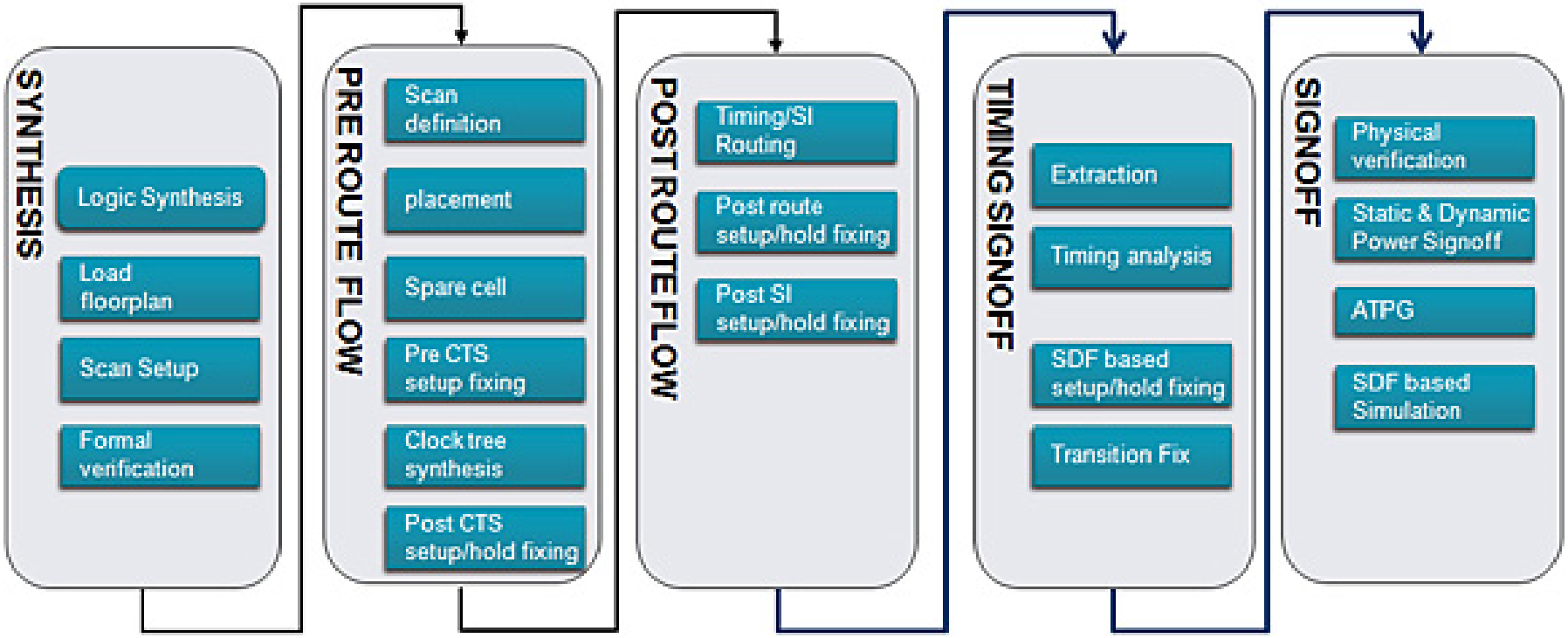
ASIC development flow:



HARDENING TECHNIQUES

Choosing the target

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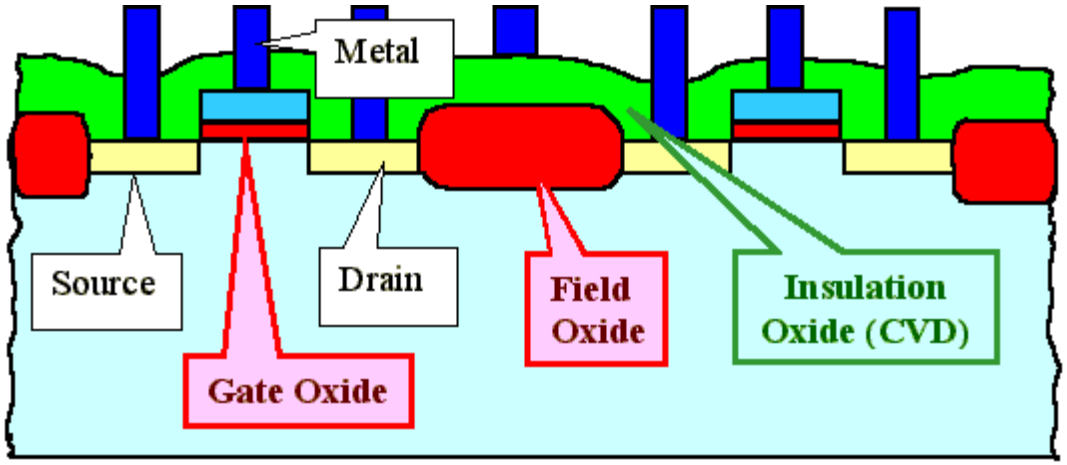
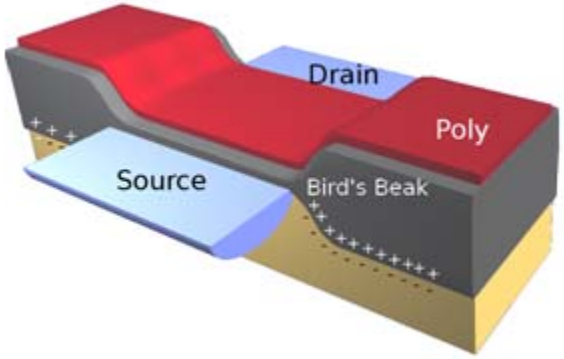
LFoundry

- Pre-design considerations
  - The process: **LF150 Lfoundry**
    - Inherent TID tolerance: up to 300krad (Thin oxide)
    - Isolated NMOS transistors (Triple Well) -> decrease SEU and SEL sensitivity
    - High Vt (low leakage) and Low Vt (High speed) devices
    - Mixed Signal Foundry
    - Isolation technique: Shallow Trench Isolation (STI)
  - The market:
    - Terrestrial, Low, Medium or Geostationary Earth Orbit (LEO, MEO,GEO)
  - The flavor
    - Low Power, High Performance, High Reliability, etc.

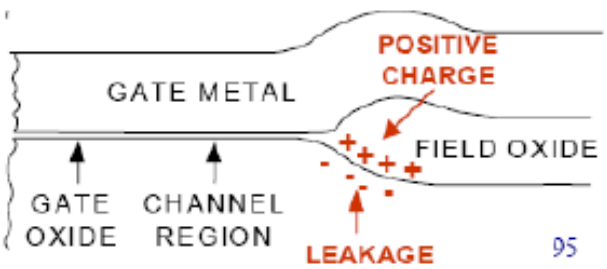
Field Oxide (FOX) and Gate Oxide (GOX):



- **Gate Oxide:** 3nm
- **Field Oxide:** 390nm



$$\Delta V_{ot} = -\frac{q}{\varepsilon_{r_{ox}}\varepsilon_o} \cdot t_{ox}^2 \cdot D \cdot k_g \cdot f_y \cdot f_{ot}$$



$\varepsilon_{r_{ox}} =$ Relative permittivity of silicon dioxide ≈ 3.9

$\varepsilon_o =$ Vacuum permittivity $\approx 8.85418 \cdot 10^{-1}$

$q =$ Electron charge $\approx 1.6021 \cdot 10^{-19}$

$t_{ox} =$ Oxide thickness

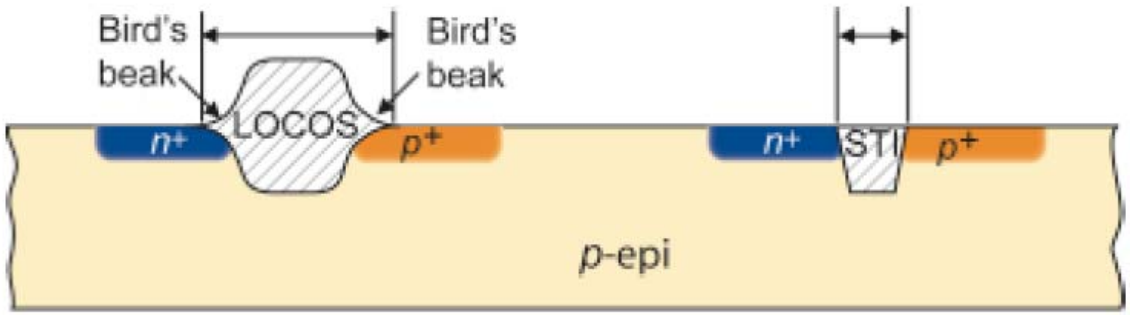
$D =$ Total ionizing dose deposited in rad

$k_g =$ Number of electron-hole pairs generated in the SiO2 $\approx 8.1 \cdot 10^{18}/cm^{-3}rad^{-1}$

$f_y =$ Probability that electron-hole pair escapes recombination ≈ 0.9

$f_{ot} =$ Hole trapping efficiency ≈ 0.2

Local Oxidation vs. Shallow Trench Isolation:



LOCAL OXIDATION (LOCOS)	SHALLOW TRENCH ISOLATION (STI)
Advantages: •Simple Fabrication Process •High Oxide Quality **Disvantages:** •So called bird's beak effect **TID behavior:** •Can become thinner in advanced nodes-> TID effect can be scaled down.	**Advantages:** •Avoid bird's beak characteristic •Prevent current leakage <250nm **Disvantages:** •Larger number of process steps **TID behavior**: •Thickness is difficult to scale down •Improves leakage effects

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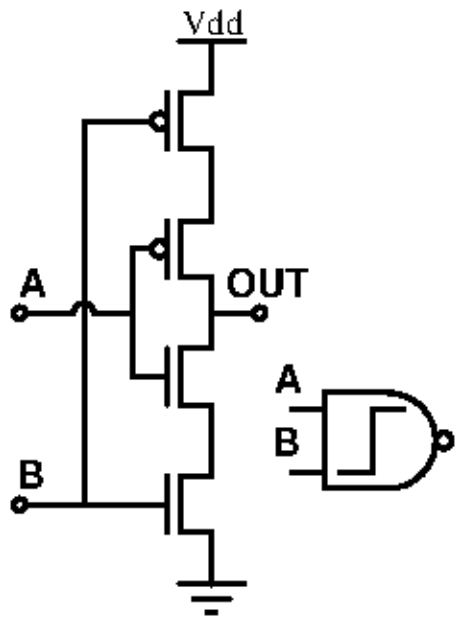
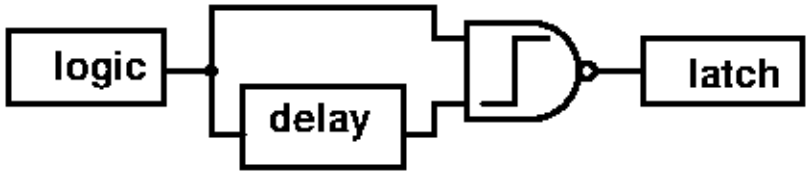
Circuit level hardening techniques:

- Total Ionization Dose (TID):
  - Minimize the use of NMOS
  - Excluding gates having more than 3 serial MOS
- Single Event Effects (SEE):
  - Junction isolated (low noise cells) are desirable (SEL inmunity)
  - DICE (Dual Interlocked Cell) topologies
  - Hardened FlipFlops(FF): Triple Modular Redundancy (TMR), Dual Modular Redundancy (DMR)
  - High capacitive nodes (↑Power, ↓Speed)
  - Code Word State Preserving (CWSP) techniques
  - Clock tree: Customized clock gate cells
  - Increase the drive strength

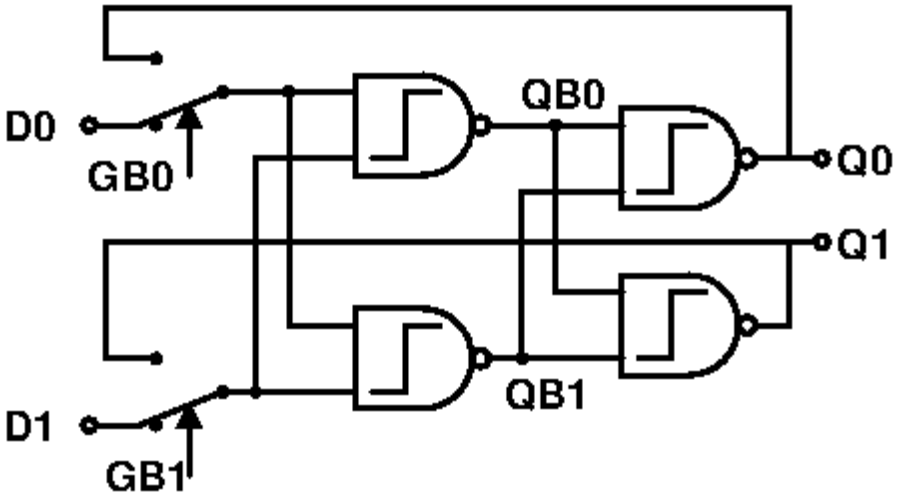
Transition Guard Gate:



Transition Guard Gate.



Guarding a latch against SET's arising in combinational logic.

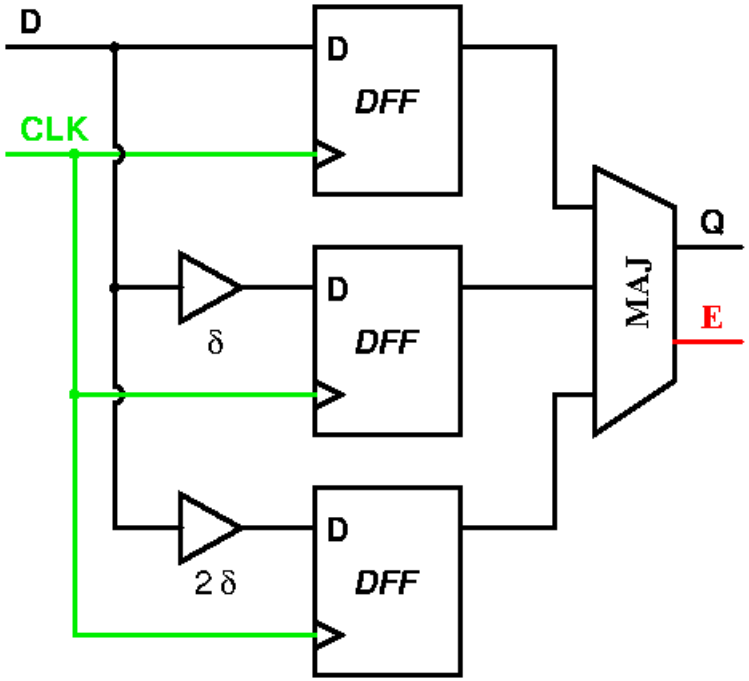


Guard-Gate storage cell using DICE configuration.

R.L. Shuler et al., "The Effectiveness of TAG or Guard-Gates in SET Suppresion Using delay and Dual-Rail Cnfigurations on 0.35um", IEEE Transacton on Nuclear Science, Dec 2006.

Temporal Redundancy (TMR Flip-Flop):

- TMR is a error correction and detection technique
- Prevents SEU(Single Event Upsets) and SET (Single Event Transient)
- Penalty: Increase of area (~4X) , power consumption and speed (slack time)
- A signal error can be easily implemented to detect errors due to SEE
- Requires some considerations in clock tree implementation

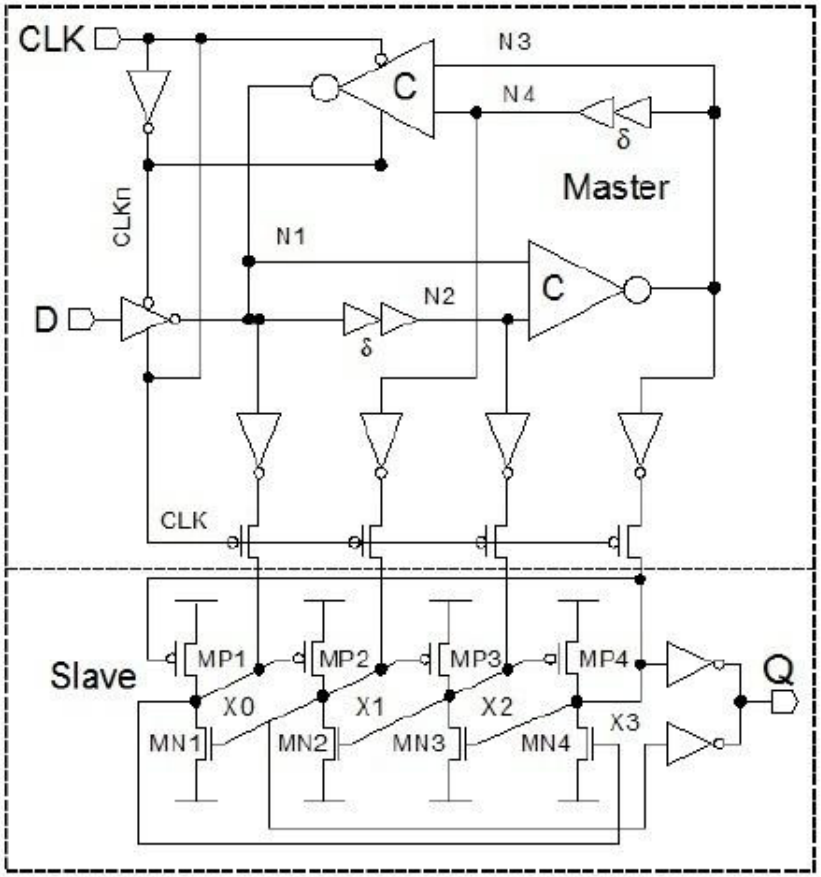


Majority voter/temporal using DICE (MTDFF):

- Nodes N1,N2, N3 e N4 have temporal redundancy
- Less area utilization in relation with TMR
- Setup and hold times **(penalty in slack time)**:

$$t_{setup} \approx 2 \cdot \delta \qquad t_{hold} = t_{holdDFF}$$

- Layout: constraints on distance between DICE nodes (charge sharing)



Temporal DICE Flip Flop Schematic

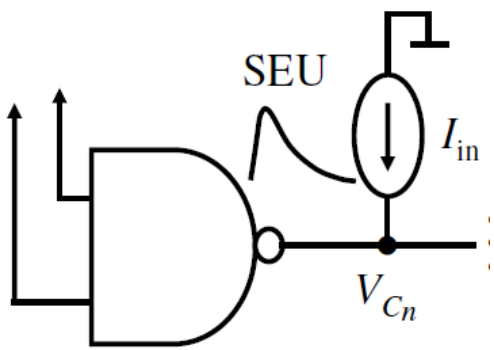
B. Matush, T. Mozdzen, L. T. Clark, "Area Efficient Temporally Hardened by Design Flip-Flop Circuits," *Presented at the 2010 NSREC, Denver, CO, July 2010.*

Hardening by Drive Strength:

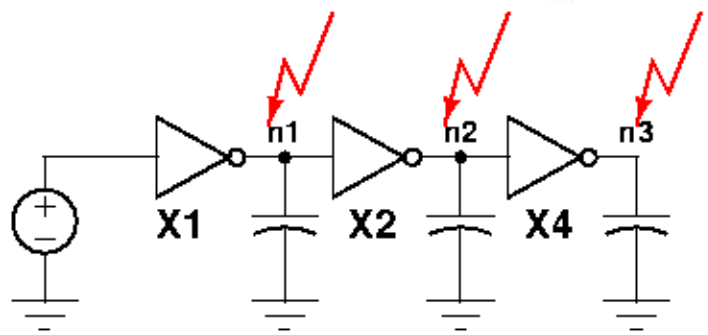
Linear Energy Transfer or **LET** is the energy deposition by length unit and depends on the material density, ρ:

$$LET = \frac{1}{\rho} \cdot \frac{\Delta E}{\Delta x} \quad \text{(In MeV.cm}^2\text{/mg or MeV/mg/cm}^2\text{)}$$

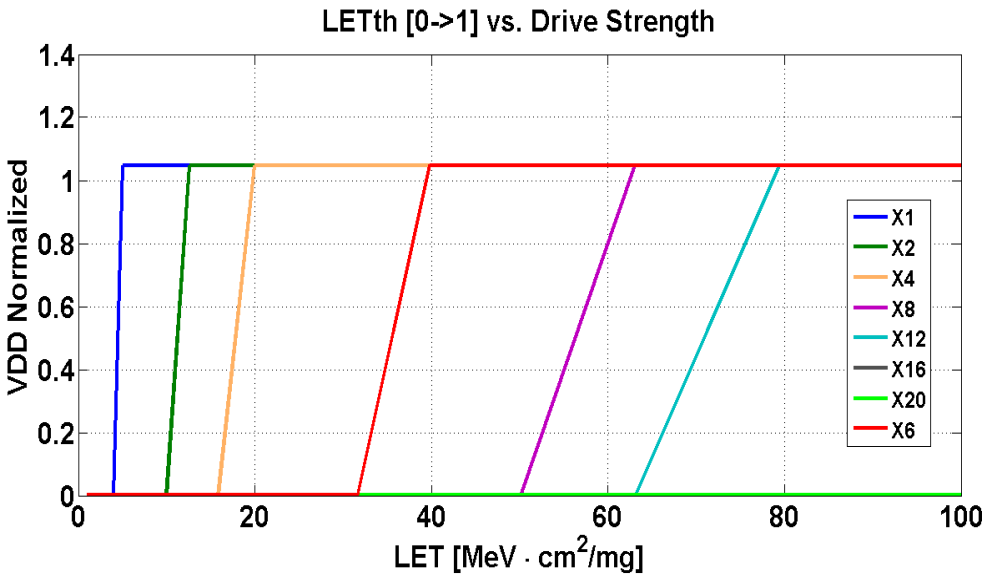
Linear Energy Transfer Threshold or **LETth** is the lowest LET required to trigger an event in the circuit.

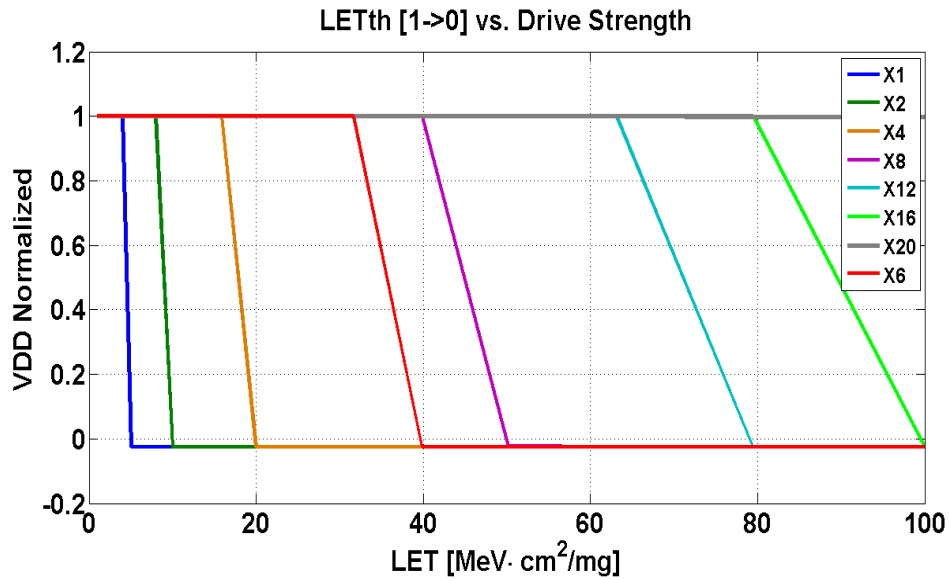


$$\frac{\partial V_{C_n}}{\partial t} = \frac{I_{in}(t) - I_D(t)}{C_n}$$



Hardening by Drive Strenght:

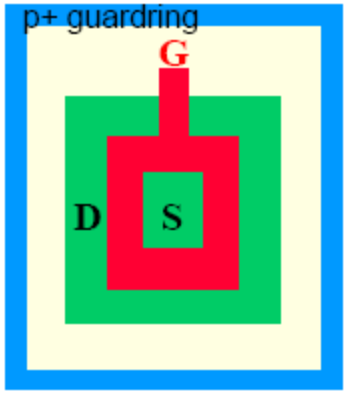


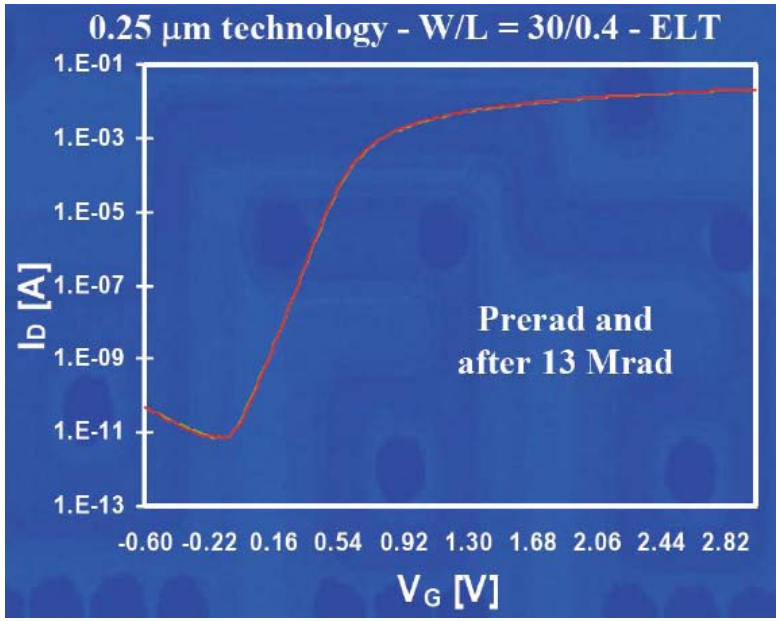


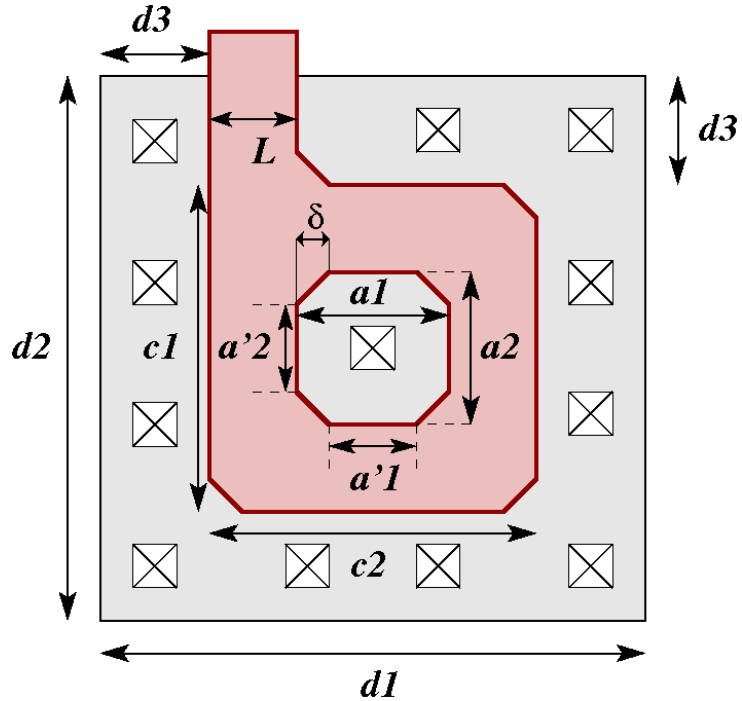
Input		BUX1	BUX2	BUX4	BUX6	BUX8	BUX12	BUX16	BUX20	Units
LETth	0->1	4.50	11.30	17.90	35.72	56.61	71.27	>100	>100	MeV.cm²/mg
	1->0	4.50	8.97	17.90	35.72	44.97	88	89.72	>100	MeV.cm²/mg

Using cells with high drive strength reduce the sensitivity of SET (Single Event Transient)!

ELT + Guard Rings = TID tolerance (mitigation)







Geometric parameters of ELT transistor

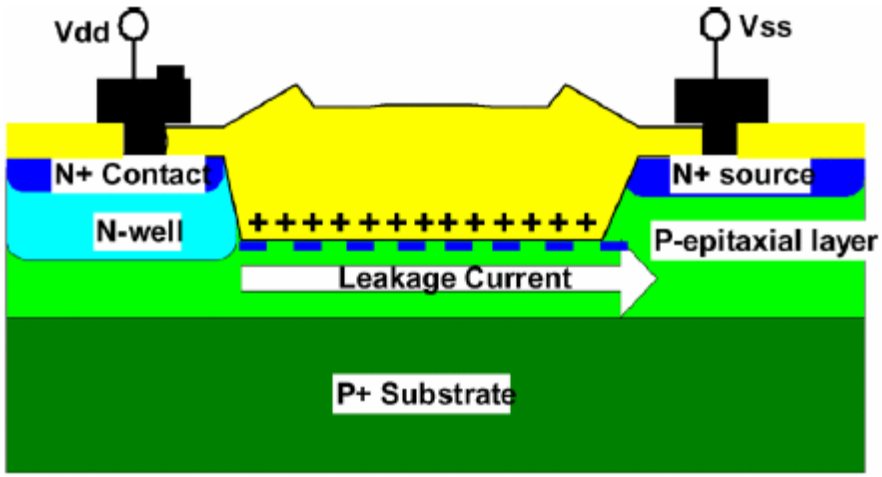
$$\left(\frac{W}{L}\right)_{eff}^{square} = 2 \cdot \left\{ \frac{2\alpha}{\ln\left(\frac{a_1'}{a_1'-2\alpha L}\right)} + \frac{2\alpha}{\ln\left(\frac{a_2'}{a_2'-2\alpha L}\right)} + \frac{4(1-\alpha)}{\Delta(\alpha)-\ln(\alpha)} + \frac{3}{2}\frac{a_1-a_1'}{2L} \right\}$$

$$\Delta(\alpha) = \frac{1}{2}\sqrt{\alpha^2+2\alpha+5}$$

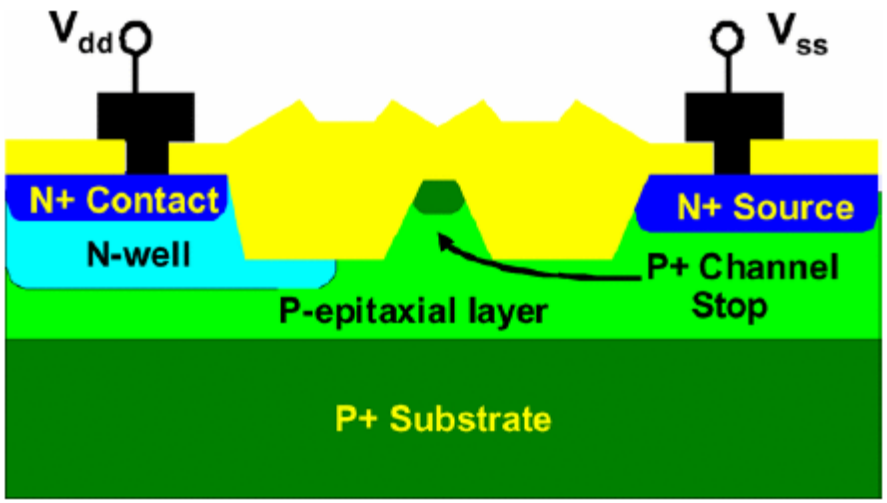
$$\delta a_1 = (a_1 - a_1')/2$$

$$\delta a_2 = (a_2 - a_2')/2$$

Guard Rings:



Radiation induced hole trapping in thick isolation field oxides can drive the parasitic field oxide transistor into inversion, resulting in leakage between adjacent devices



A p+ channel stop in the field-oxide isolation to reduce interdevice leakage

HARDENING TECHNIQUES
Layout Level

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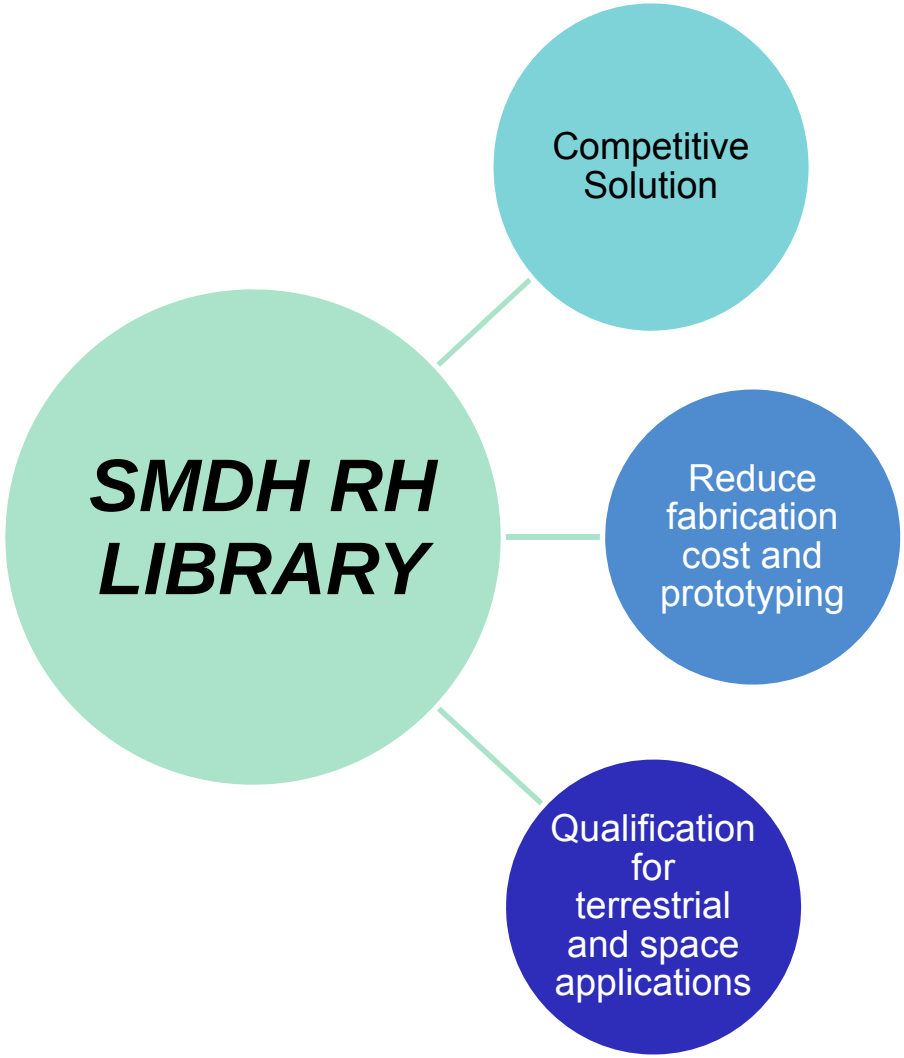
- Summary of layout level techniques:
  - ELT or dogbone transistor when necessary.
  - Guard Rings.
  - Large number of contacts.
  - N-WELL and BULK contacts close to P-N junction.
  - Large supply metal lines.
  - Use separate n-wells for each PMOS device - Multi Bit Upset (MBU).
  - Place guard bands with additional bulk contacts between adjacent devices.

Goals:



- Low mass and high performance solution
- Low power and low area implementation

- Use commercial process
- High reliability
- Portability

- Wider range of application Aerospace/Terrestrial

SMDH RH LIBRARY
Library Development

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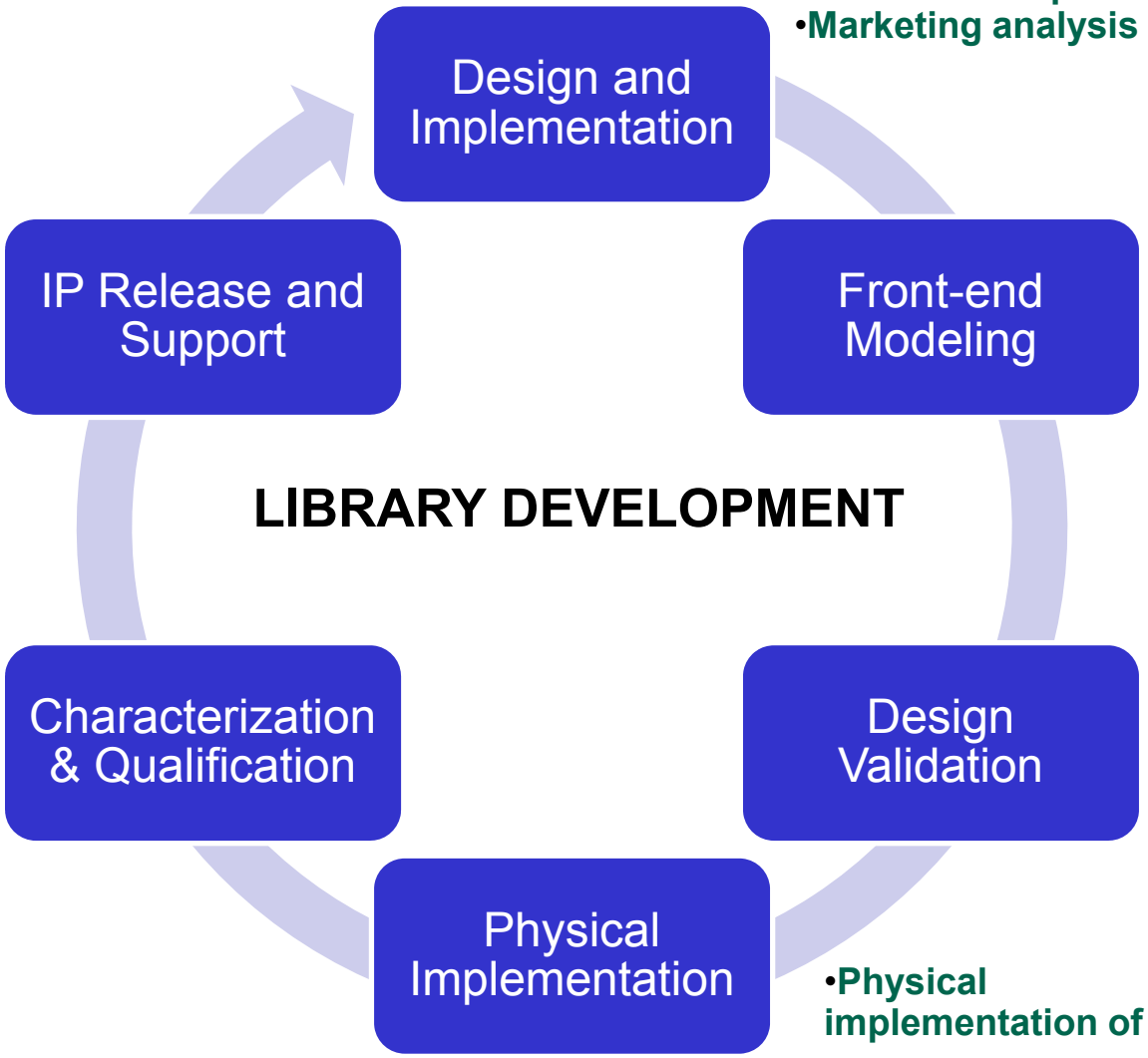


- Feasibility analysis
- Schematic Capture
- Marketing analysis

- Behavioral model development
- Schematic Capture

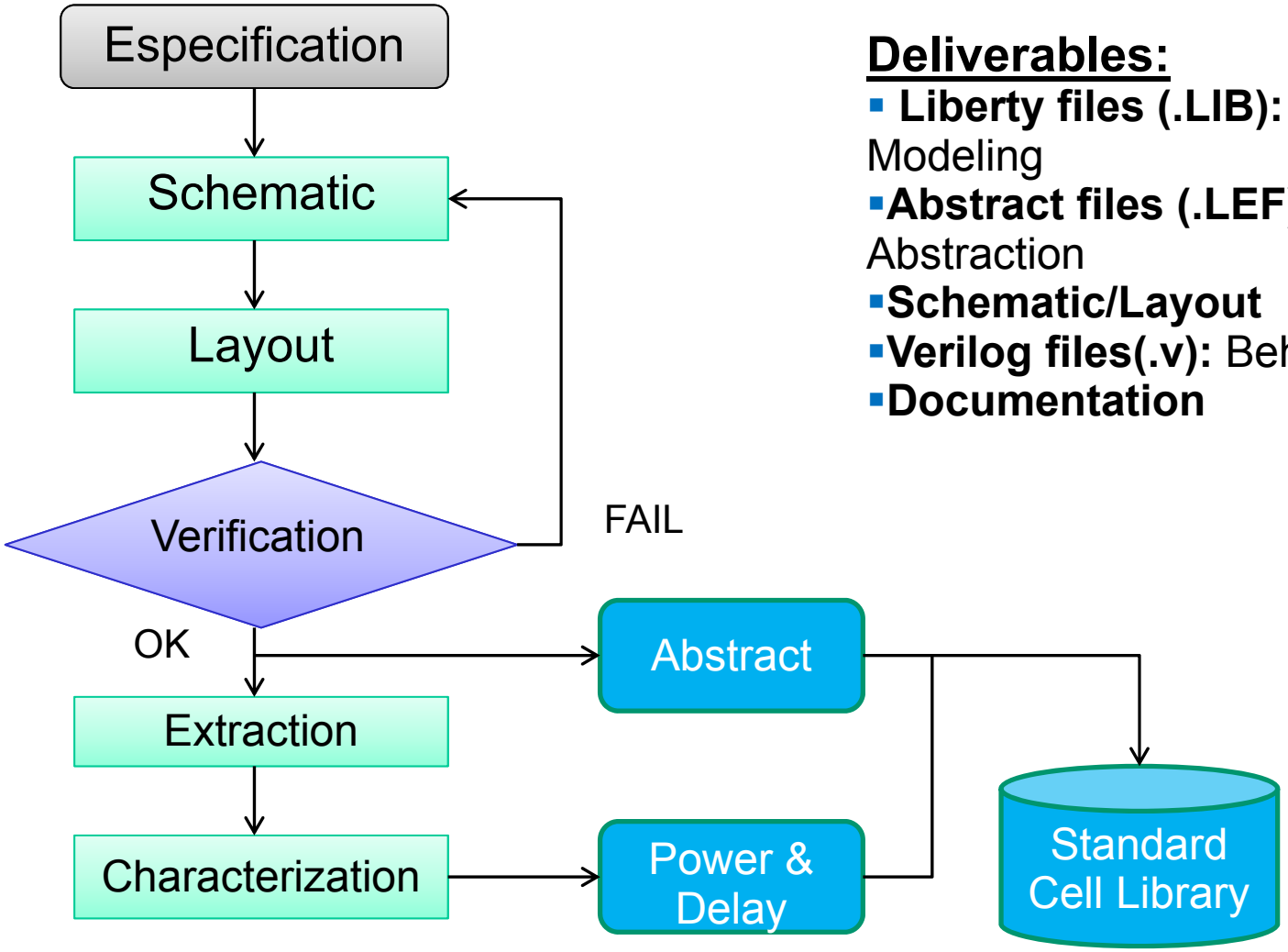
- Functional verification of design

- Physical implementation of cells

- Characterization
- Data validation
- Qualification

- Validation of all IP views
- Technical support

Standard cell development flow:

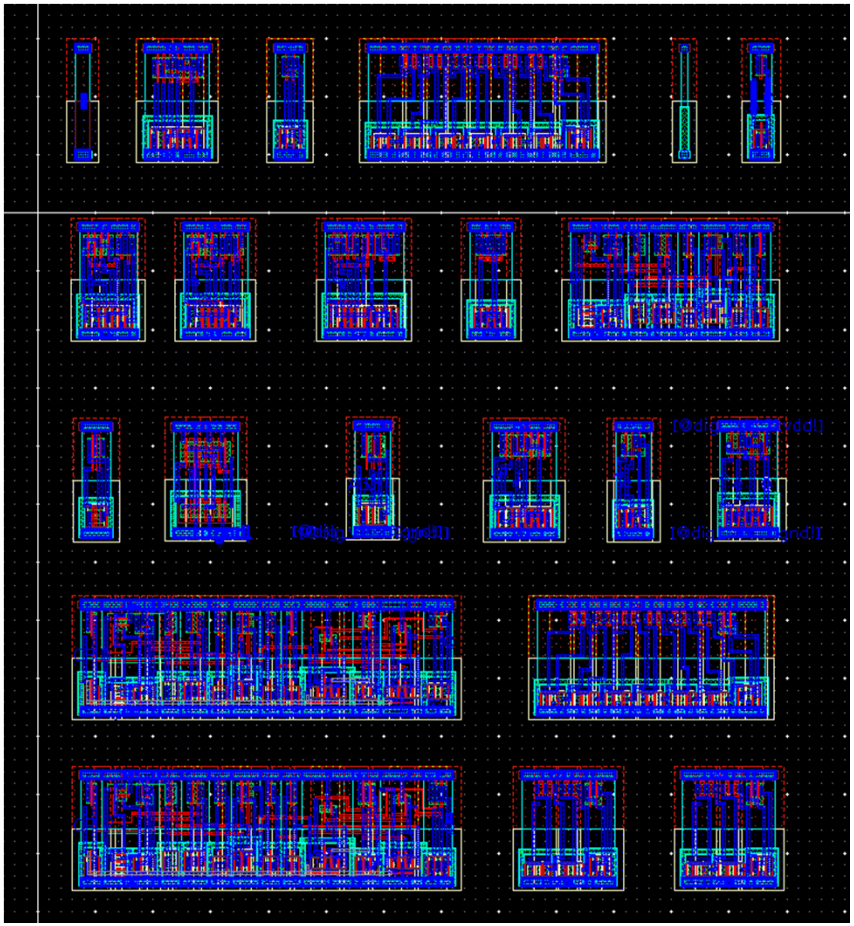


Deliverables:

- **Liberty files (.LIB):** Power/Timming Modeling
- **Abstract files (.LEF):** Physiclal Abstraction
- **Schematic/Layout**
- **Verilog files(.v):** Behavioral models
- **Documentation**

Characteristics:

- Process: 150nm LFoundry 6 Metal Layer CMOS Technology
- Version 1.0 released in 2010
- ~ 76 cells (Combinational + Sequential + Glue cells)
- General applications <300krad
- Available drive strenghts: X1, X2 and X4
- No ELT transistors due intrinsic good response of LF150 process
- RH hardened DFFs and latches
- Multiple delays configurations for SET/SEU tolerance
- Silicon proven



SDMH RH Library in Lfoundry 150nm process

SMDH RH LIBRARY
Combinational cells

Cell name	Description
AND2RH_X1, AND2RH_X4	AND cells (X1 and X4)
BUFRH_X1, BUFRH_X2	BUFER cells
DELAY_100, DELAY_400 DELAY 1200	100ps, 400ps and 1.2ns DELAYs cells
INRH_X1, INRH_X4	INVERTER cells (X1 and X4)
LOGICRH0, LOGICRH1	TIE HIGH and LOW cells
MUX2RH_X1, MUX2RH_X2, MUX2RH4	MUX cells (X1, X2 and X4)
NAND2RH_X1, NAND2RH_X4, NAND3RH_X1	2-inputs and 3-inputs NAND cells (X1, X4)
NOR2RH_X1, NOR2RH_X4	2-inputs NOR cells (X1 and X4)
OA21RH_X1,OA21RH_X4	ORAND cells (X1 and X4)
OR2RH_X1, OR2RH_X4	2-inputs OR cells (X1 and X4)
TRIPLEVOTER	Triple voter cell
XNOR2RH_X1, XNOR2RH_X2, XOR2RH_X1, XOR2RH_X2	XNOR and XOR cells (X1 and X2)

List of combinational cells available in SMDH RH Library.

SMDH RH LIBRARY
Sequential Cells

Sequential cells available in different delays configurations:

Cell name	Description
DF100RH_X1, DF100RH_X4	D-type FF with 100ps of delay (X1 and X4)
DF400RH_X1, DF400RH_X4	D-type FF with 400ps of delay (X1 and X4)
DF1200RH_X1, DF1200RH_X4	D-type FF with 1200ps of delay (X1 and X4)
DICERH_X1	DICE Latch (X1)
DELAY_GUARD_GATE_100_X1 **DELAY_GUARD_GATE_400_X1** **DELAY_GUARD_GATE_400_X4** **DELAY_GUARD_GATE_1200_X1** **DELAY_GUARD_GATE_1200_X4**	Delay guard gates with 100ps, 400ps and 1200ps delay.
LH100RH_X1, LH100RH_X4	Latch with 100ps of delay (X1 and X4)
LH400RH_X1, LH400RH_X4	Latch with 400ps of delay (X1 and X4)
LH2000RH_X1, LH2000RH_X4	Latch with 2ns of delay (X1 and X4)

List of sequential cells available in SMDH RH Library.

SMDH RH LIBRARY
Electrical Characteristics

Cell name	Area[um²]	Power [uW/MHz] *	Delay [ps]*
INVRH_X1	17.07	0.017	0.016
BUFRH_X1	22.76	0.026	0.046
DF400RH_X1	324.42	0.078	0.162
LH400RH_X1	187.82	0.034	0.120
MUX2RH_X1	45.53	0.036	0.081
NAND2RH_X1	22.76	0.014	0.046
NOR2RH_X1	22.76	0.019	0.041

* Measured @ 0.01ns transition time and Cload=1fF

Electrical parameters of some cells in SMDH RH Library.

NanoSatC-BR1
Overview

- Decision to create the NANOSATC-BR Program and to built the NANOSATC-BR1 a 1U CubeSat (2008);
- Opportunity of Research (publications) and Technology Development.
- First missions suggested by INPE scientists.
- Work for the NANOSATC-BR Program start in 2009.

NanoSatC-BR1
Overview

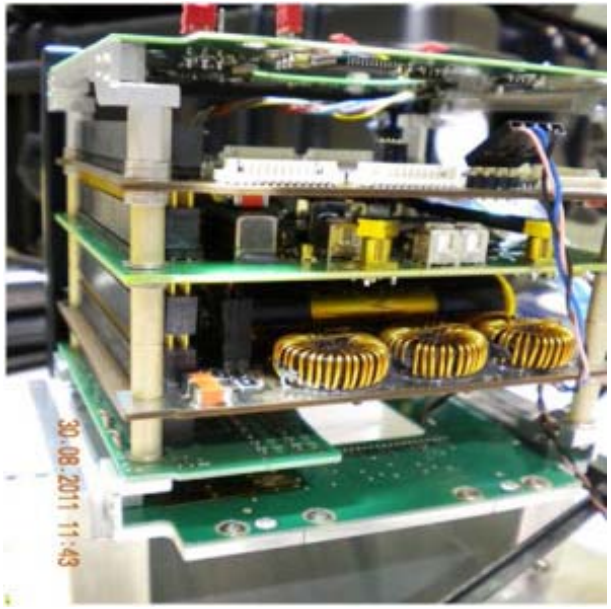
Santa Maria Design House

Development strategy:

- To develop the mission rather than the platform.
- Start with payload development, software and operation.
- Re-engineering to develop the platform subsystems.
- To create an industry in Brazil for this class of satellite.
- To bring technology from abroad and incorporate it through the industry – joint ventures.

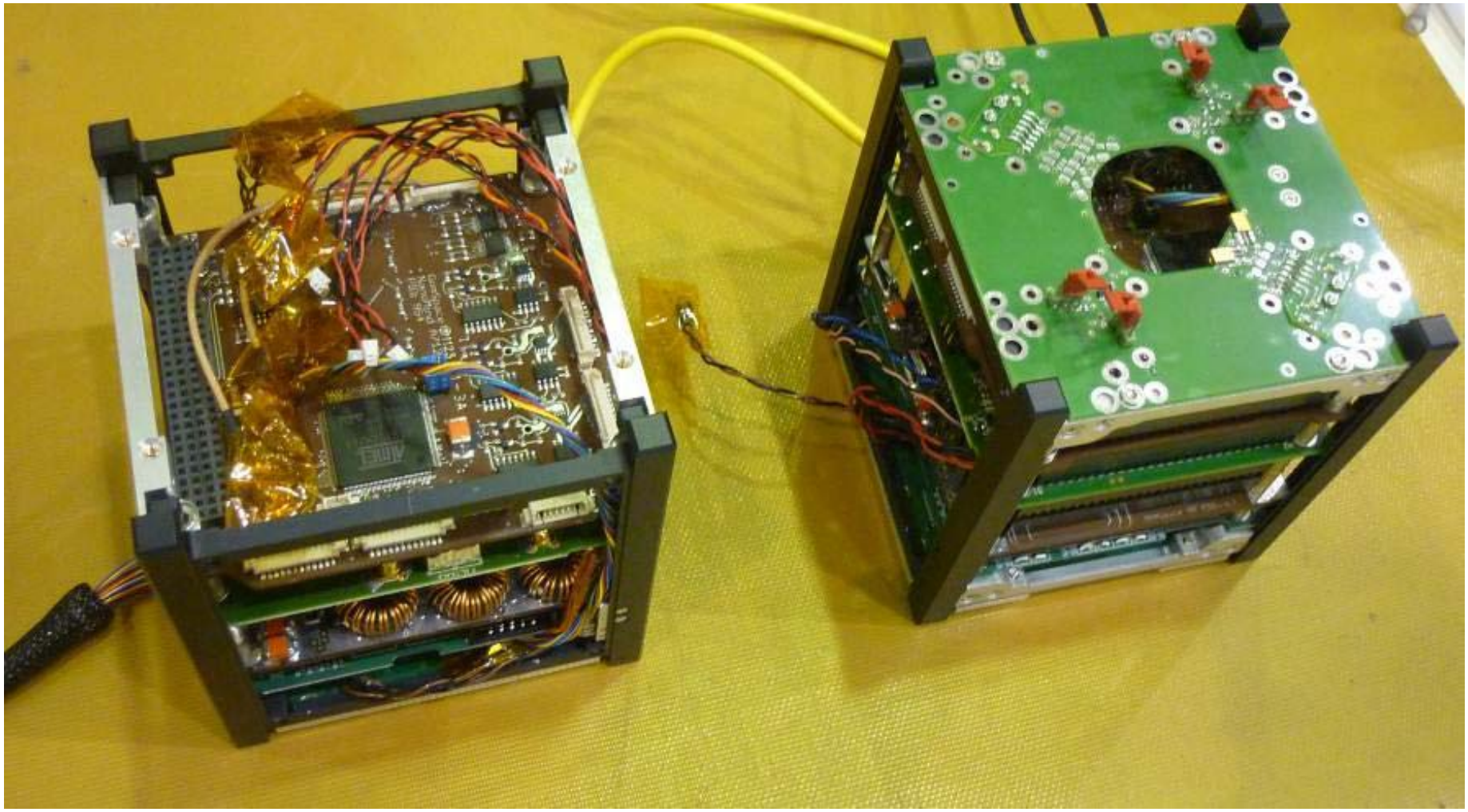
NanoSatC-BR1
Overview

- NanoSatC-Br1 was launched on 19th July 2014
- It is the first Brazilian CubeSat project
- The 1U CubeSat carries an ISIS U/V transceiver with 1200 bps FM AX.25 UHF command uplink and a 9600 bps BPSK downlink on 145.865 MHz.



NanoSatC-BR1

NanoSatC-BR1
Overview



NanoSatC-BR1
Payload Board

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- The three-axis magnetometer with a resolution of 15nT (XEN-1210)

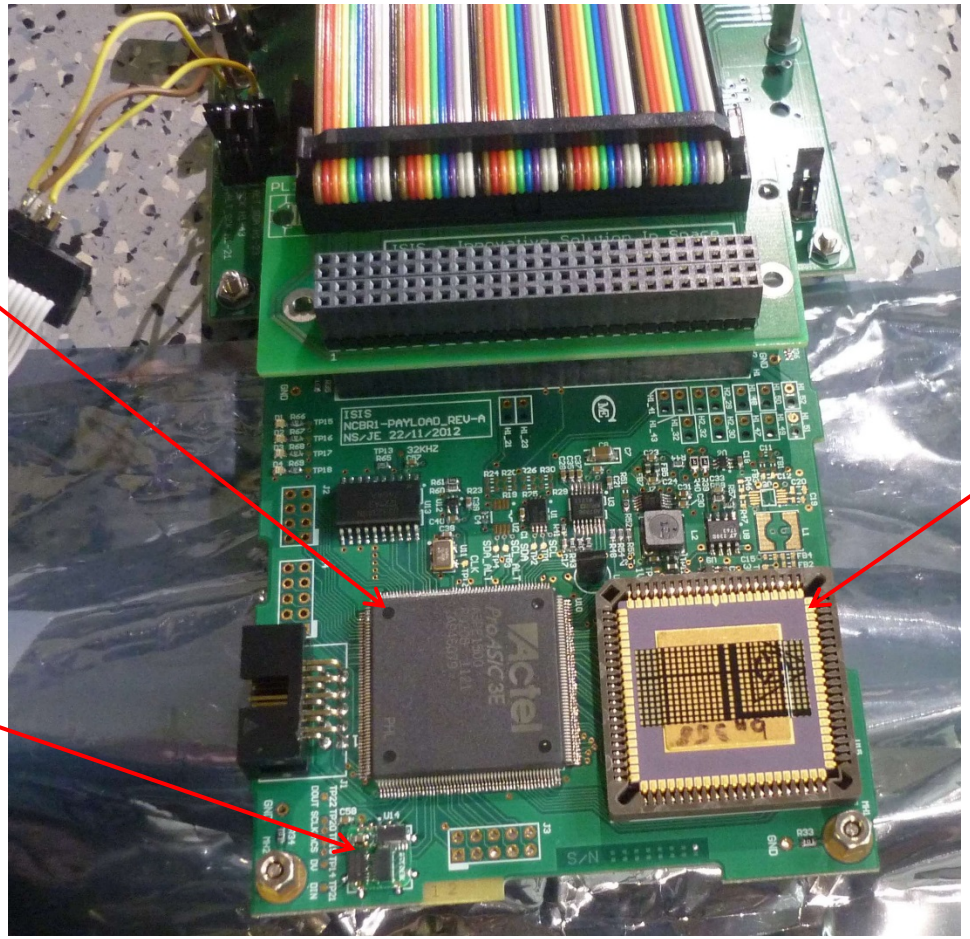
  Earth Magnetic Field intensity measurements.

- FIELD PROGRAMMABLE GATE ARRAY - ProASIC3 A3PE1500-PQ208 FPGA

  Programmed algorithm for fault tolerance – UFRGS

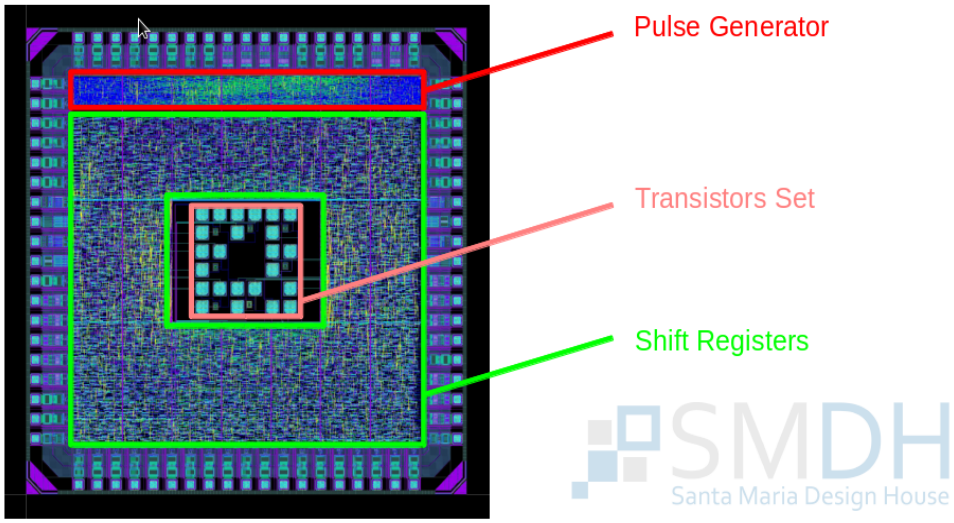
- <u>RHDRV Library and ON-OFF Switch</u>

NanoSatC-BR1
Payload Board



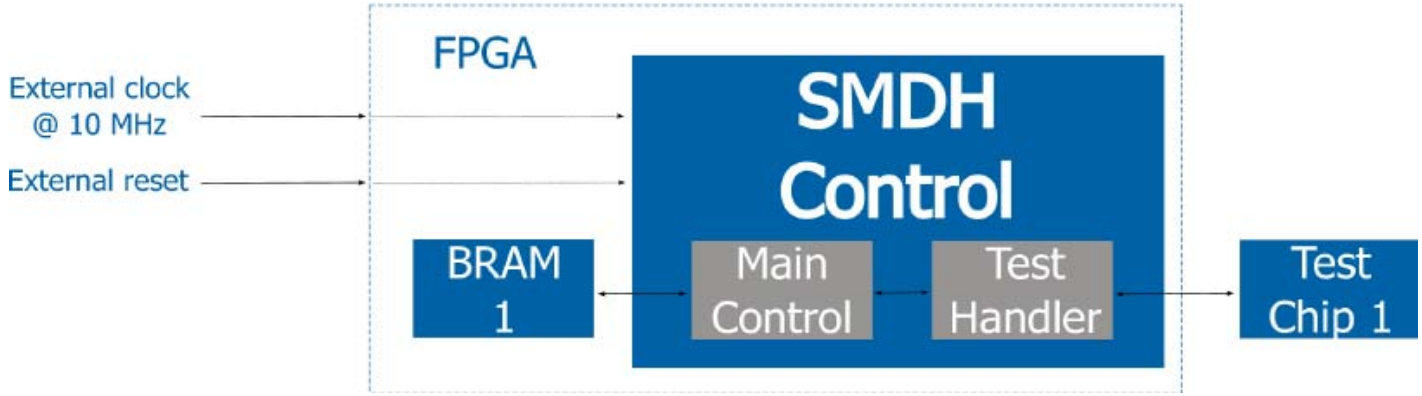
NanoSatC-BR1
Prototype

- **Pulse generator:** Low Voltage – High Power Command (LV-HPC) defined in Spacecraft Discrete Interfaces (ECSS) from European Space Agency (ESA).
- **Shift Registers (SR):** 10 SR with different configurations and delays to evaluate SEE tolerances.
- **Transistors Sets:** Isolated transistors both tolerant to radiation such as non-tolerant.



Die of the prototype used in NanoSatC-Br1

NanoSatC-BR1
On-Flight Test

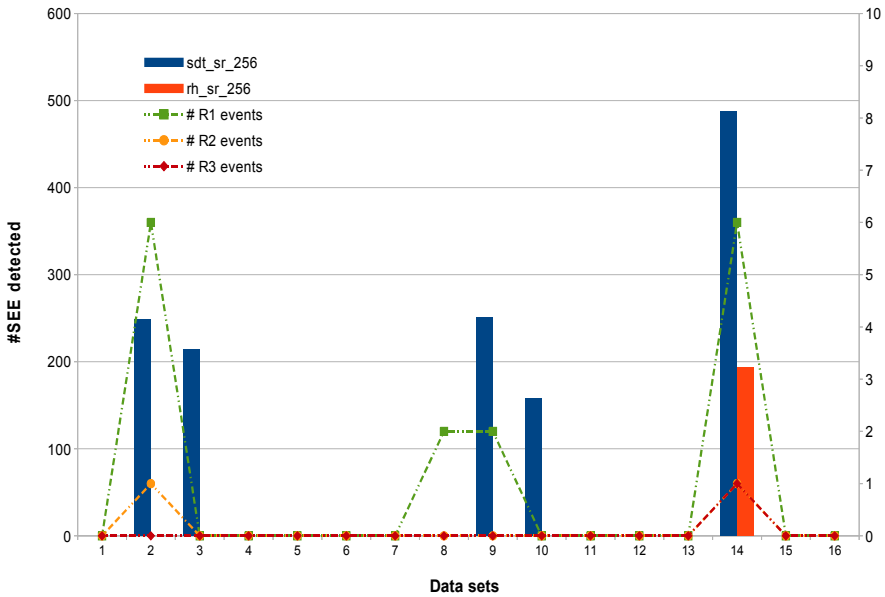


SMDH test handler

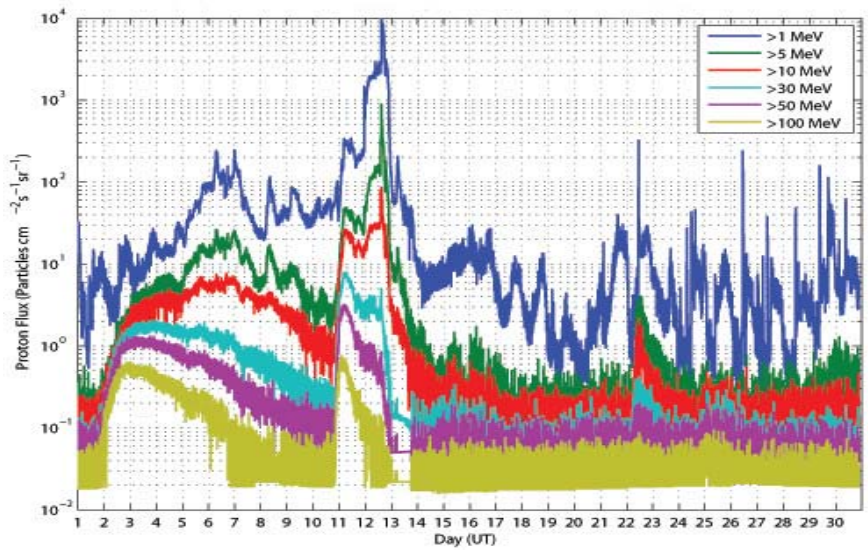
Test	Bits response	Execution Time (us)
PG_ACTIVE	4	1920
PG_NO_PULSE	4	1920
PG_PULSE_OFF	4	1920
SR_PATTERN_GEN_ALT_256	5	1024
SR_PATTERN_GEN_ALT_1024	5	4096
Total	22	10880

Test execution list

RH Library LF150 proved a tolerance to solar energetic particles of energies up to 100MeV.



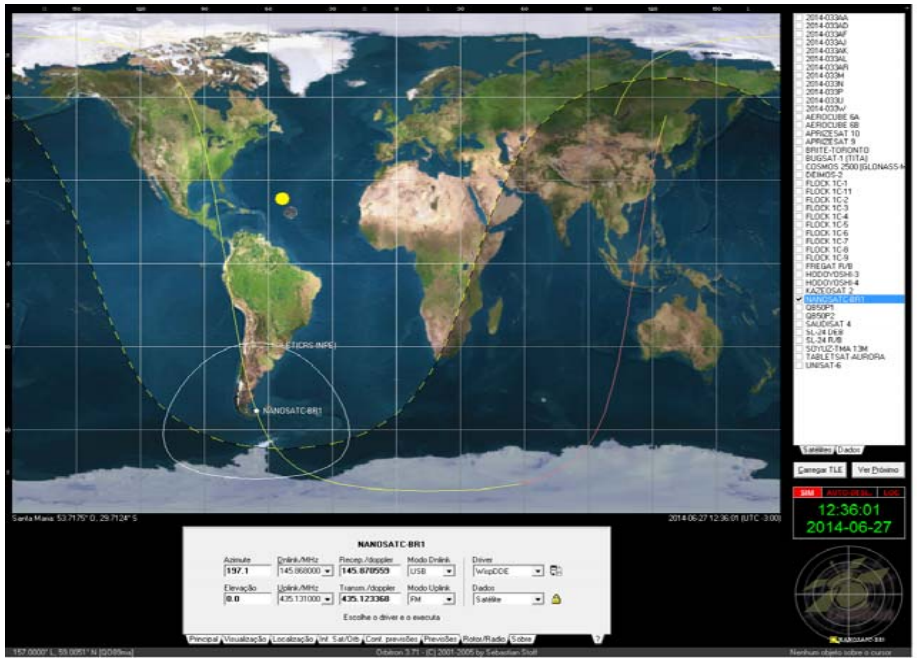
Number of erros detected
RH structure vs. Standard structure



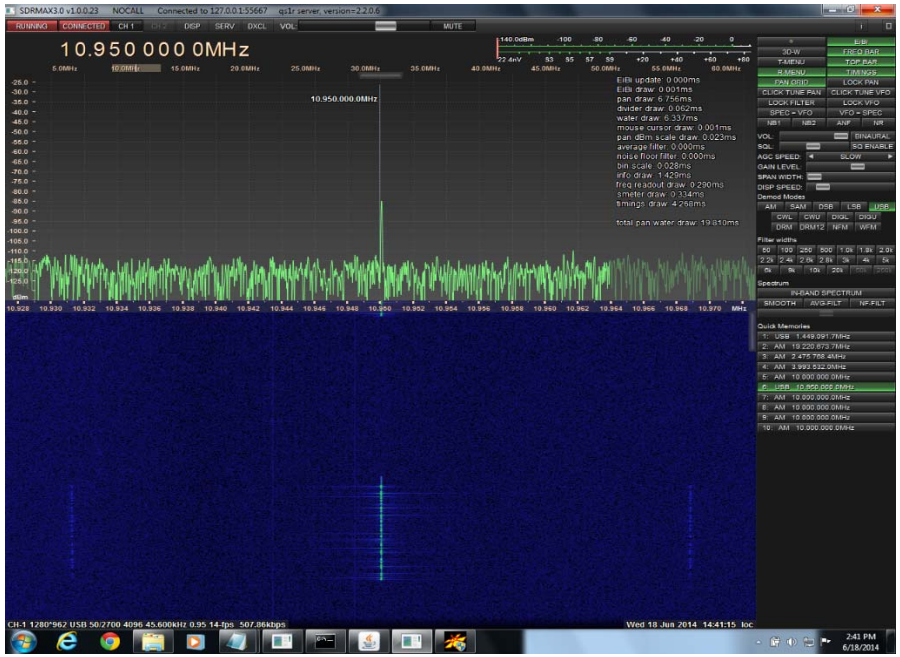
Solar activity measured
by proton activity

NanoSatC-BR1
Tracking & Telemetry

Orbitron: NANOSATC-BR1 Tracking



NanosatC-BR1: Morse Code (CW) Beacon.



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GDSII sent on **6th March 2015** (XFAB XH018):

- **Telecommand (LV-HP):**
  - Over Current/Voltage Protection
  - False/Double Pulse Detection
  - Digital controller tolerant to TID e SEE
- **Shift Registers**
  - Shift Registers with and without temporal redundancy
- **Test structures**
  - 17-stages ring oscillator
  - Frequency divider/buffer
  - TID tolerant pads

NanoSatC-BR2
Prototype

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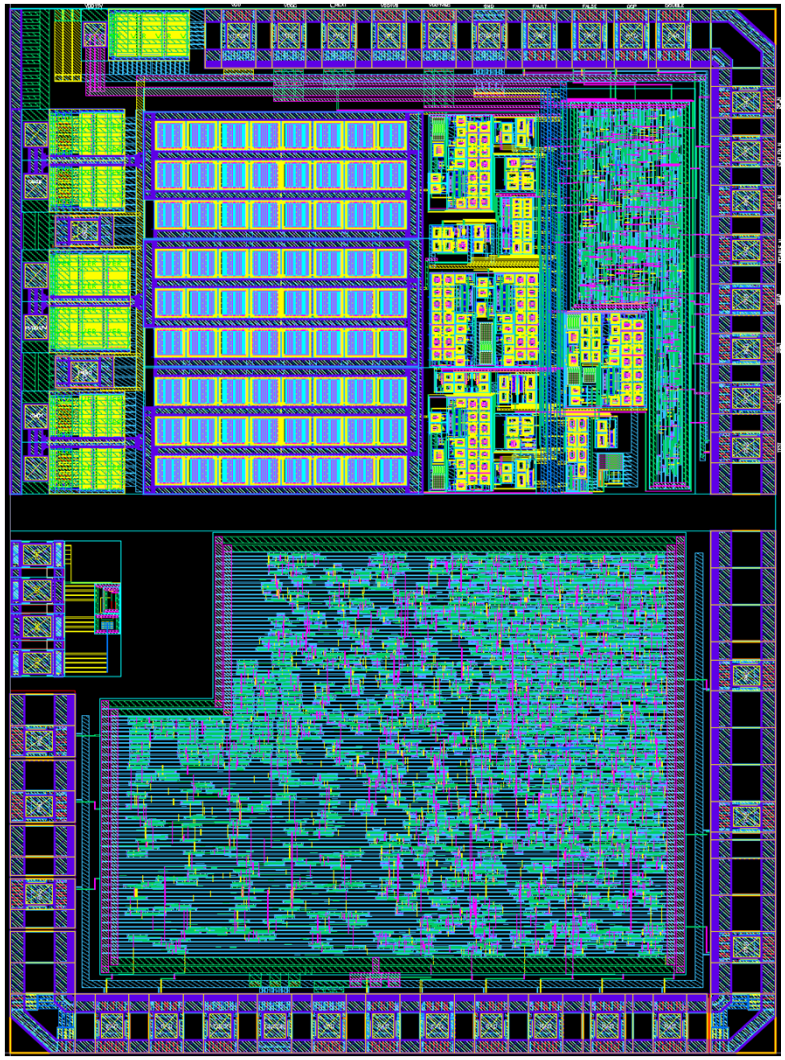
- **LVHP Telecommand:**
  - Area:1.9mmX1.4mm
  - Digital controller: 153 DFF
- **Shift-Registers**
  - ~ 9k instances
  - 1028FF+ 5k inverters + Clock tree
  - Current consumption: ~440uA @1MHz
  - Area:1.9mmX1.5mm
- **Ring oscillator**
  - Area: 0.27mmx0.36mm



Die of NanoSat-CBR2 prototype

SMDH RH Library: The future

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- Qualification of digital cells
- Radiation hardened I/O cells library
  - Digital cells
  - LVDS cells
- Expand the digital cell portfolio
- Radiation hardened microprocessor ZR16RH08
- SRAM tolerant to SEE using EDAC
- SRAM compiler

THANKS ..